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Analysing the effects of the EFT/B immunity test

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Outline

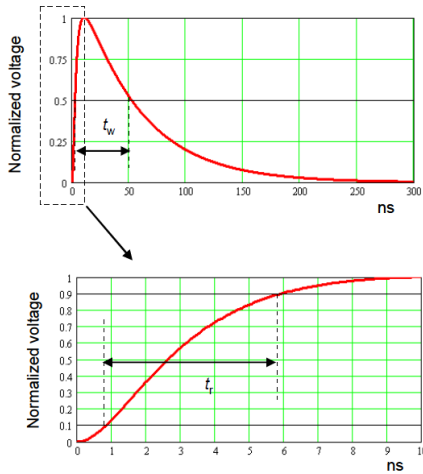


- The EFT/Burst test and its generator
- An experimental setup to determine coupling and its Spice model
- Some results of the experiment and comparing it to the model
- Another experimental setup, its model and results
- Conclusion and insights

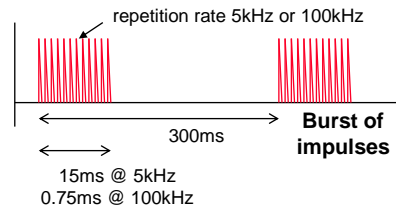
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The IEC 61000-4-4 ideal waveform

A single pulse...



in a burst of 75 pulses

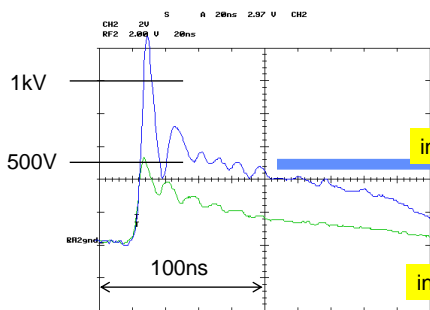
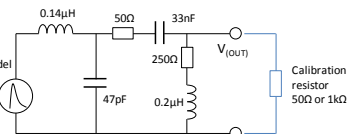


Tolerances:
 rise time $t_r = (5 \pm 1,5)$ ns
 Into 50 ohms:
 pulse width $t_w = (50 \pm 15)$ ns
 peak voltage, half indicated level $\pm 10\%$
 Into 1000 ohms:
 pulse width $t_w = 50$ ns, tolerance -15 ns to $+100$ ns
 peak voltage, 0.95 indicated level $\pm 20\%$

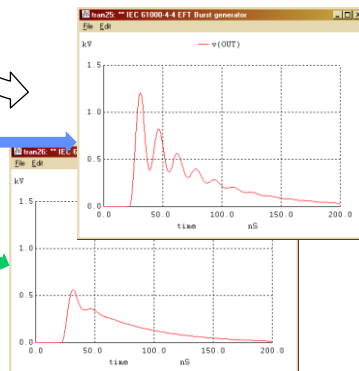
The actual generator output

The model

For 1kV output:
 Transient voltage source, Spice model
 EXP(0.1400 20ns 4ns 8ns 56ns)

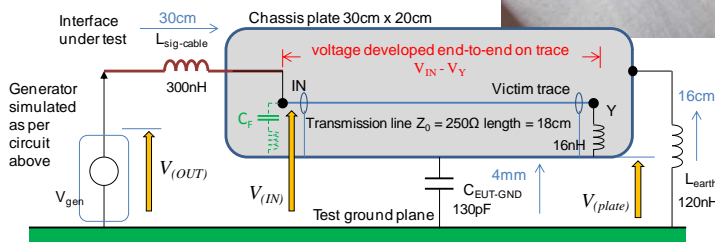
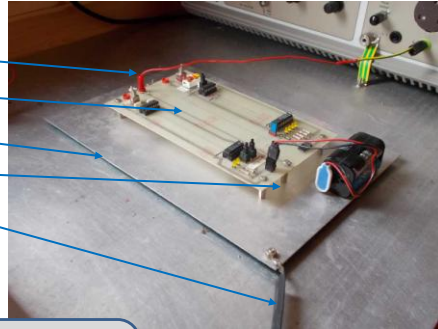


Actual calibration waveform



The first experiment: trace over chassis

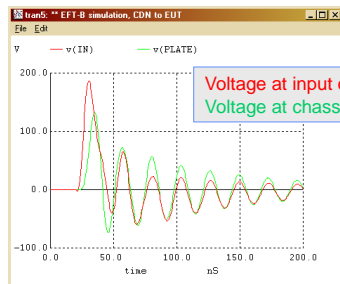
- 30cm injection wire
- PCB trace
- Chassis plate 4mm above ground plane
- Trace connected to plate
- 16cm strap from plate to ground plane



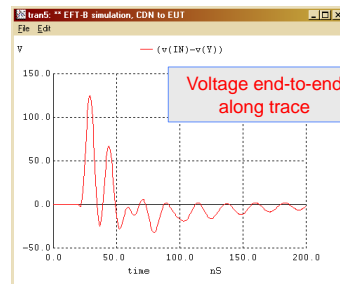
The model

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Comparison of model vs. actual waveforms

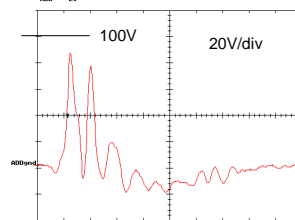
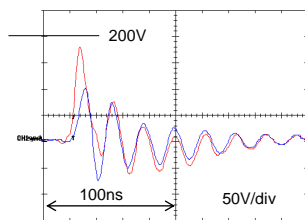


Voltage at input of trace
Voltage at chassis plate



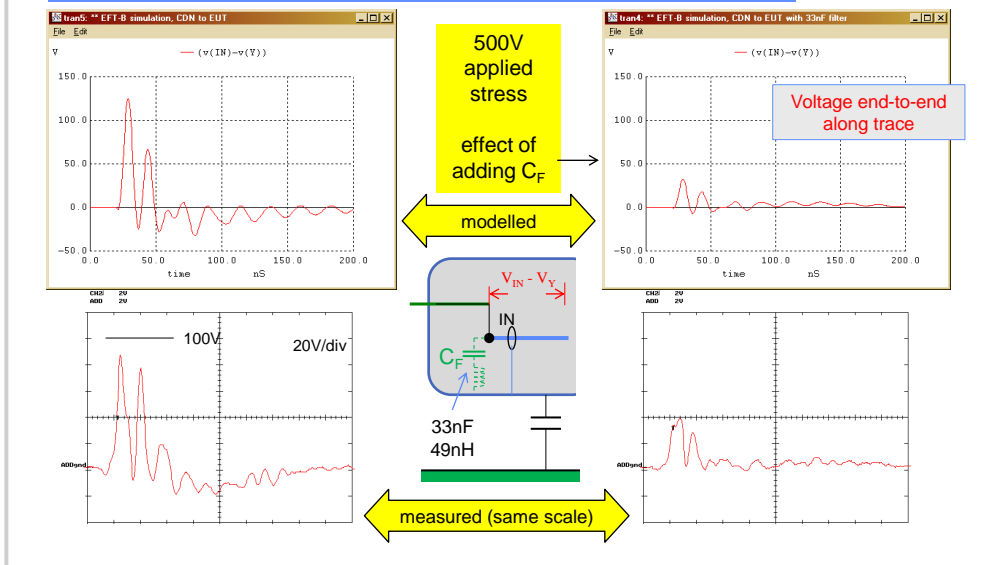
Voltage end-to-end
along trace

500V applied stress
modelled
measured



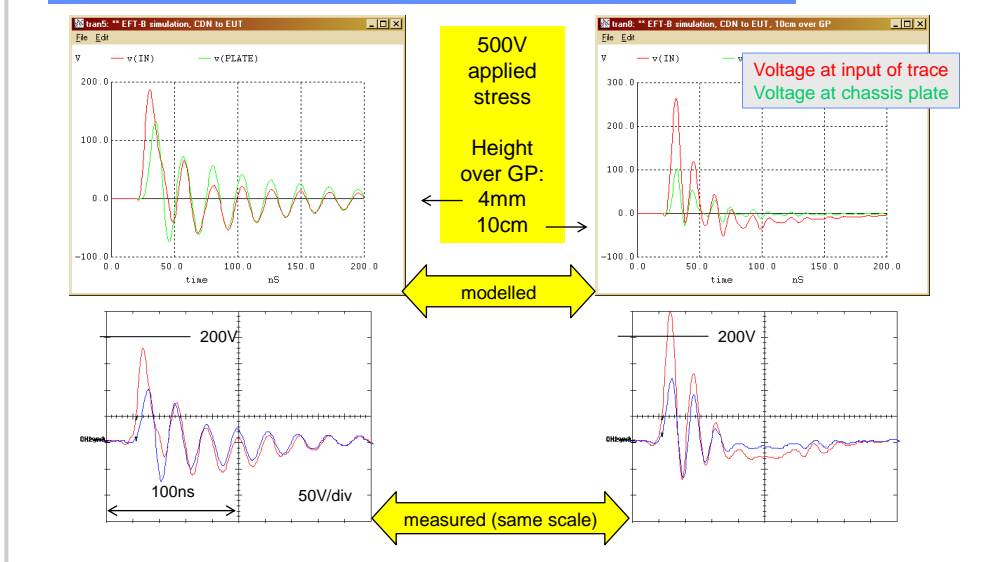
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Comparison with/without filter capacitor



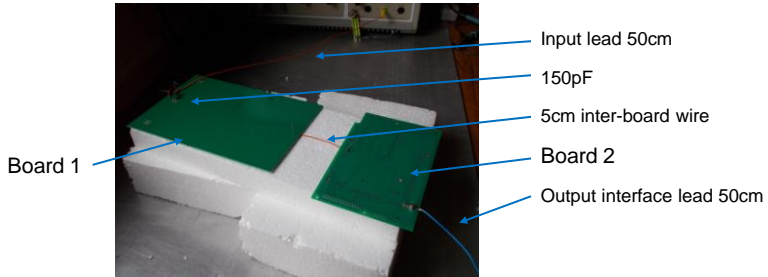
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Comparison of height above test ground plane

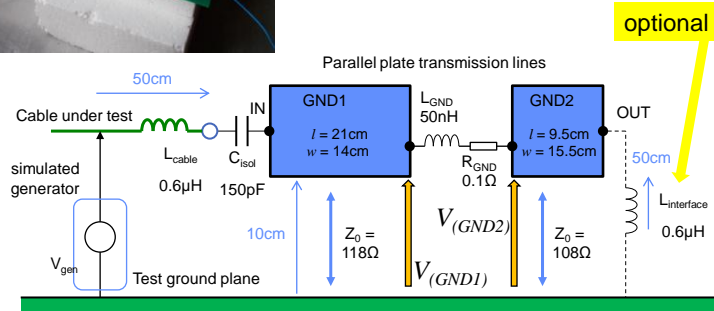


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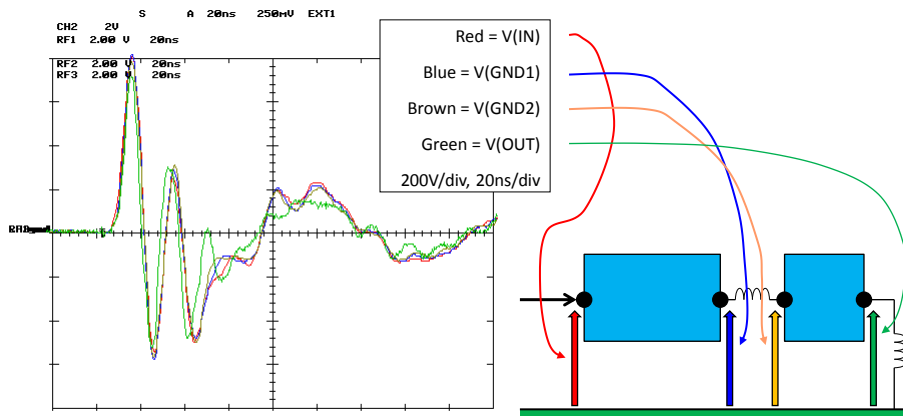
The second experiment: 2 boards, no chassis



The model

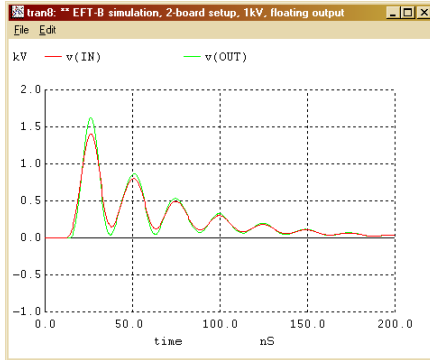


Example actual waveforms

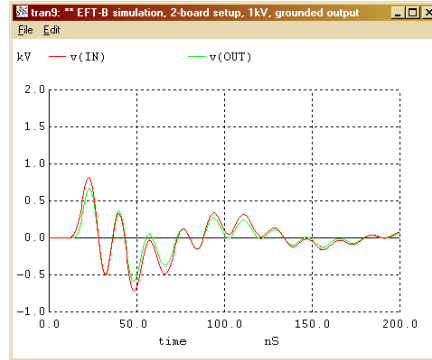


+1kV stress, OUT interface grounded through 50 cm

Model analysis – IN/OUT voltages



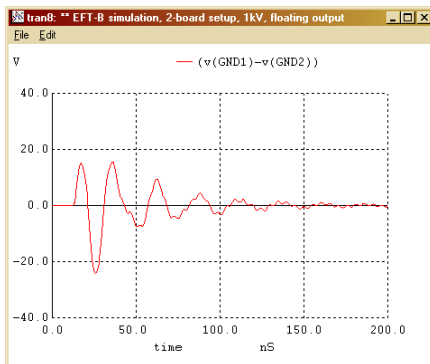
OUT interface: Floating



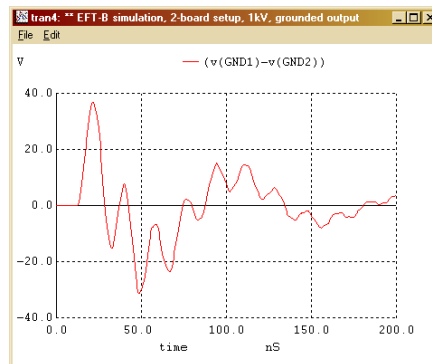
Grounded through 50 cm

+1kV stress, IN and OUT voltages

Model analysis – inter-board voltages



OUT interface: Floating



Grounded through 50 cm

+1kV stress, GND1 – GND2 voltages

Conclusions and insights – the test

- The actual waveforms and levels on the EUT during an EFT/B test are nothing like the idealised stress:
 - they are modified by the parasitic impedances of the various structures, including the connecting cables and the presence and proximity of the test ground plane
 - they have a large and variable-frequency ringing component
- External interfaces other than the one being tested have a significant effect on the coupling, and must always be carefully controlled in the test plan

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Conclusions and insights – modelling

- Consider the *electrical* behaviour of *mechanical* components:
 - not the circuit schematic, rather the structures and wires that are present as components themselves
 - draw up an equivalent circuit which shows their interconnections in the context of the external test setup
- Modelling this circuit can show the actual waveforms at critical points in the structure
- The model can evaluate options for improving immunity, as long as the parasitics are included

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END

Thanks for your attention!

A more detailed description can be found at
www.elmac.co.uk/Papers.html